In the Claims:

Claim 1 (currently amended): A DC driver circuit coupled to a tip/ring line, said DC driver circuit comprising:

a first capacitor coupled to a first switch, said first switch coupled to an amplification circuit, said amplification circuit being coupled to said tip/ring line;

an RC circuit coupled to a second switch, said second switch coupled to said amplification circuit, said RC circuit comprising a second capacitor and at least one resistor;

said first switch being closed and said second switch being closed during a make state to cause said amplification circuit to draw current from said tip/ring line;

said first switch being open and said second switch being open during a break state to prevent said amplification circuit from drawing current from said tip/ring line;

a third switch having a first terminal coupled to a voltage source and a second terminal coupled to said first capacitor, said third switch being closed during said break state to precharge said first capacitor to enable said first capacitor to transfer charge onto said second capacitor at initiation of said make state;

wherein said RC circuit, said first switch, and said amplification circuit share a common node such that a rate of discharge of a voltage at said common node is controlled by changing at least one value of said second capacitor and said at least one resistor, thereby changing a rate at which a DC loop current at said tip/ring line changes.

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Claim 2 (canceled).

Claim 3 (previously presented): The DC driver circuit of claim 1 wherein said second capacitor has a first terminal coupled to said amplification circuit and a second terminal coupled to ground.

Claim 4 (previously presented): The DC driver circuit of claim 3 wherein said first capacitor has a first capacitance value that is substantially greater than a second capacitance value of said second capacitor.

Claim 5 (previously presented): The DC driver circuit of claim 1 wherein a resistor of said RC circuit has a first terminal coupled to said amplification circuit and a second terminal coupled to ground.

Claim 6 (original): The DC driver circuit of claim 1 wherein said amplification circuit comprises an op amp coupled to a first transistor.

Claim 7 (original): The DC driver circuit of claim 1 wherein said amplification circuit comprises an op amp coupled to a first transistor, said first transistor being coupled to a second transistor.

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Claim 8 (original): The DC driver circuit of claim 6 wherein said first transistor is coupled to said tip/ring line, wherein said first transistor is caused to draw current from said tip/ring line in said make state, and wherein said first transistor is prevented from drawing current from said tip/ring line in said break state.

Claim 9 (original): The DC driver circuit of claim 7 wherein said first and second transistors are coupled to said tip/ring line, wherein said first and second transistors are caused to draw current from said tip/ring line in said make state, and wherein said first and second transistors are prevented from drawing current from said tip/ring line in said break state.

Claim 10 (original): The DC driver circuit of claim 1 wherein said tip/ring line is coupled to a modem.

Claim 11 (currently amended): A circuit for reducing a peak voltage at a selected line, said circuit comprising:

at least one transistor driving said selected line;

said at least one transistor being driven by a first capacitor when said circuit is in a make state;

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said at least one transistor being driven by an RC circuit when said circuit is in a break state, said RC circuit comprising a second capacitor and at least one resistor;

said RC circuit reducing said peak voltage at said selected line when said circuit transitions from said make state to said break state;

a voltage source coupled to said first capacitor during said break state to precharge said first capacitor to enable said first capacitor to transfer charge onto said second capacitor at initiation of said make state;

wherein said RC circuit, a first switch, and an amplification circuit share a common node such that a rate of discharge of a voltage at said common node is controlled by changing at least one value of said second capacitor and said at least one resistor, thereby changing a rate at which a DC loop current at said selected line changes.

Claim 12 (original): The circuit of claim 11 wherein said selected line is a tip/ring line.

Claim 13 (original): The circuit of claim 11 wherein said at least one transistor is driven by an op amp.

Claim 14 (original): The circuit of claim 13 wherein said op amp is driven by said first capacitor when said circuit is in said make state.

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Claim 15 (previously presented): The circuit of claim 11 wherein said first switch causes said at least one transistor to be driven by said first capacitor when said circuit is in said make state.

Claim 16 (original): The circuit of claim 15 wherein a second switch causes said at least one transistor to be driven by said RC circuit when said circuit is in said break state.

Claim 17 (previously presented): The circuit of claim 13 wherein said second capacitor has a first terminal coupled to said op amp and a second terminal coupled to ground.

Claim 18 (previously presented): The circuit of claim 17 wherein said first capacitor has a first capacitance value that is substantially greater than a second capacitance value of said second capacitor.

Claim 19 (currently amended): The circuit of claim 16 further comprising a third switch having a first terminal coupled to asaid voltage source and a second terminal coupled to said first capacitor, said third switch being closed during said break state to precharge said first capacitor.

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Claim 20 (previously presented): The circuit of claim 13 wherein said at least one resistor of said RC circuit has a first terminal coupled to said op amp and a second terminal coupled to ground.

Claim 21 (original): The circuit of claim 12 wherein said tip/ring line is coupled to a modem.

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